Impact of Annealing on the Resistivity of Ultrafine Cu Damascene Interconnects

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Abstract

The influence of different annealing conditions on the electrical resistivity of copper damascene interconnects with lateral dimensions down to sub-50 nm was studied. Different thermal treatments after copper plating as well as annealing processes in addition to the final anneal step were carried out in order to study the microstructural change of copper damascene lines. It was found that rapid thermal annealing (RTA) at high temperatures (600°C) leads to an enlargement of the Cu grains by a factor of 2 for wide lines, whereas a significant impact of annealing on the median grain size of ultrafine lines was not observed. This is attributed to the geometrical limitation of the grain growth process. As a result, the size effect in Cu nano-interconnects which is mainly determined by grain boundaries acting as scattering sites for electrons cannot be reduced significantly by using thermal treatments.

Introduction

Efficient on-chip communication means high-speed signal transmission with minimal propagation delay. As technology scales down to smaller dimensions an increasing disparity between gate and interconnect signal delay (τ=RC) appears. Besides the conductor geometry the RC product depends on the properties of the intermetal dielectric (IMD) and the conductor material: the dielectric constant k and the electrical resistivity ρ. In this work in particular the electrical resistivity of ultrafine Cu damascene lines for application in future metallization systems is studied.

If electrical current flows, charge carriers are scattered at internal and external surfaces and interfaces on their way through a polycrystalline metal conductor. Due to electron scattering effects the electrical resistivity increases with shrinking line dimension. This is known as size effect in thin Cu lines /1-4/. A physical model, which combines both electron scattering effects at internal and external scattering sources, was developed in order to interpret the electrical size effect in interconnects. The key parameters are p, the probability of specular scattering at the surface, λ, the mean free path of

![Fig. 1: Electrical resistivity of Cu damascene lines with different lateral dimensions down to 43 nm. A physical model combining scattering effects at internal (I) and external (II) surfaces is in excellent agreement with the experimental data.](image-url)
the conduction electrons, $R_{gb}$, the reflection coefficient at grain boundaries and $G_{50}$, the median grain size. With a parameter set of $p=0.5$, $\lambda=40$ nm, $R_{gb}=0.45$ and $G_{50}/G_{40}$, where $G_{50}$ denotes the interconnect line width, the model is in excellent agreement with the experimental data (Fig. 1). It was found that the main contribution is scattering at internal interfaces like grain boundaries. Thus, an increase of grain size leading to a reduced number of grain boundaries and, hence, scattering sites can be very useful in helping to overcome the size effect related resistivity problem. As reported in /5/, the median grain size decreases with decreasing interconnect line width and $G_{50}$ is in the order of the lateral dimension of the interconnect line. As a result, grain size engineering to increase the median grain size in Cu nano-interconnects for future metallization systems is desirable in order to reduce grain boundaries.

**Experimental**

Sub-lithographic copper damascene interconnects embedded in SiO$_2$ with feature sizes down to 50 nm and below were fabricated using a spacer technique for intermetal dielectric (IMD) patterning /6/. The subsequent metallization processes include barrier (10 nm) and seed layer deposition (15 nm and 30 nm, respectively) and the filling of the trenches with electroplated Cu (350 nm and 700 nm, respectively). After plating of Cu the structures were subjected to a post-plating anneal in order to enhance recrystallization. One sample set was annealed in N$_2$/H$_2$ ambient using a standard furnace at 175°C for 50 min and 150°C for 30 min, respectively. For comparison rapid thermal processing (RTP) at different temperatures was applied to other samples. Very short heating and cooling ramps to temperatures between 250°C and 600°C are typical for RTA. The ramp-up rate of the RTA tool is between 10°C and 30°C per second and the ramp-down rate is about 2°C/s. For $T<400$°C a thermocouple attached to a graphite susceptor is used to control the temperature. More details about the RTA tool used are given in /7/. Finally the excess metal was removed in a chemical mechanical polishing process and then the Cu lines were passivated with a Si$_3$N$_4$/SiO$_2$ bi-layer. For electrical contacting the pad windows were opened and Al was deposited. In addition some samples were annealed with RTA or subjected to long term storage at 275°C.

4-point measurements were used to measure the electrical resistance at two temperatures in order to evaluate the resistivity of the Cu lines at room temperature without analyzing the cross-sectional Cu area as described in /3/. Using the bulk value of the linear temperature coefficient of the resistance of copper, $\alpha_0$, and Matthiessen’s rule stating that the size effect related contribution to the total electrical resistivity is temperature independent the electrical resistivity can be calculated using

$$\rho(T) \cdot \alpha = \frac{\partial \rho(T)}{\partial T} = \frac{\partial \rho_0(T)}{\partial T} = \rho_0(T) \cdot \alpha_0$$

(1)

$$\rho(T_1) - \rho_0(T_1) = \rho_0(T_2) - \rho_0(T_2)$$

(2)

For grain size analysis the passivation of the lines was removed. Atomic force microscopy (AFM), focused ion beam (FIB) analysis and transmission electron microscopy (TEM) were used to visualize the Cu grains in damascene lines down to 50 nm. The micrographs were analyzed and the length of the identified Cu grains were counted by the median line-intercept method /8/. The length of each grain along a line in the center of the inlaid copper was quantified. Twin boundaries, which are planar defects in the crystal structure and do not act as scattering sites for electrons, were not included for the grain size distribution.
Results

Based on theoretical predictions the size effect related resistivity increase can be reduced by enlarging the median grain size $G_{50}$ or reducing the reflection coefficient $R_{gb}$. For example doubling $G_{50}$ of 45 nm wide Cu damascene lines ($G_{50}$=90 nm) would result in only a half of the resistivity increase compared to a typical $G_{50}$=45 nm. In Fig. 2 the dependence of the grain boundary scattering contribution to the electrical resistivity on the median grain size is plotted for different $R_{gb}$. With decreasing grain size the resistivity increases. Furthermore, a reduction of $R_{gb}$ leads to a significant lower resistivity.

The microstructure of Cu lines is mainly determined by the post-plating annealing process and a final anneal step. In this study an additional final anneal after processing and several modifications of the post-plating anneal after electrochemically depositing of Cu were applied.

Additional Final Anneal

In addition after processing the Cu lines were subjected to several thermal treatments to enhance a second grain growth process. A long term storage at 275°C (>3400 h) in a furnace at ambient atmosphere was applied. The resistance was measured after different periods of time. No changes in the resistance (Fig. 3a) and, thus, in the grain size were found. TEM micrographs of 65 nm wide Cu lines with and without annealing are compared in Fig. 3b.

In addition, some samples were subjected to RTA after the final anneal step in order to increase the temperature and to keep the heating and cooling cycles as short as possible. RTA at 500°C, 600°C and 700°C was applied for 10 min in forming gas atmosphere (N2/H2). For temperatures higher than 500°C these treatments result in formation of hillocks in copper lines (Fig. 4).

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Fig. 2: Influence of the median grain size $G_{50}$ and the reflection coefficient $R_{gb}$ on the electrical resistivity.

Fig. 3: Resistance measurements after different periods of time (a) and TEM micrographs (b) after long term annealing at 275°C. The numbers in the legend in (a) denote the line widths.
Post-Plating Anneal
The main recrystallization process during the annealing step after copper electroplating was varied in order to optimize the grain growth process. Instead of the standard post-plating anneal at 175°C for 50 min in forming gas using a tube furnace the samples were subjected to relative low temperature RTA to stimulate and optimize the recrystallization process prior to chemical-mechanical polishing. The grain size for two annealing parameter sets was analyzed based on AFM micrographs taken after post-plating annealing and compared to the microstructure of plated Cu using standard annealing (Fig. 5). We have observed that grains become larger as process duration or, in particular, temperature is increased.

As a result, the median grain size can be enlarged by a factor of more than 2 by RTA processing after plating. For higher temperatures (>500°C) outgrowths at grain boundaries were found. This is attributed to impurities, which accumulate at the grain boundaries before annealing and grow out of the copper film along the grain boundaries at high temperatures (Fig. 5c).

Finally, the microstructure was studied after chemical-mechanical polishing in order to investigate the line width dependence of the median grain size. Based on FIB analysis the microstructure of Cu lines was studied. In Fig. 6 a typical FIB micrograph of a 700 nm wide line is shown. The median grain size, \( G_{50} \), was quantified for samples with standard post-plating annealing and RTA at 600°C and plotted versus the line widths.

![Fig. 4: Hillock formation (indicated by arrows) due to RTA after final annealing.](image)

![Fig. 5: Grain size distributions (a) obtained for various thermal treatments performed after Cu plating. The median grain size \( G_{50} \) is indicated for each sample. AFM micrographs (b, c) were used to quantify the median grain size for different annealing conditions.](image)
As expected $G_{50}$ decreases with decreasing line width for all annealing processes. For lines with aspect ratios (ratio between height and width) smaller than 1 the median grain size, $G_{50}$, of 1200 nm wide lines subjected to RTA is a factor of 2 larger compared to those annealed with the standard process. The difference between $G_{50}$ of the samples subjected to standard annealing and $G_{50}$ of annealed samples using RTA is less significant for smaller line widths and increasing aspect ratios (Fig. 7a). This could be also found for the electrical resistance measurements. The resistivity was calculated using Eq. (2). In Fig. 7b the size effect of Cu damascene lines is compared for the two annealing processes, RTA and standard annealing. For the case of AR>1 where the lateral dimension is small compared to the trench height the microstructure of all Cu lines is comparable independent of the annealing process. The steeper slope of the resistivity curve of RTA samples can be attributed to an increasing reflection coefficient due to outgrowths at grain boundaries shown in Fig. 5a. However, in particular two parameters mainly determine the electrical resistivity: the grain size and the reflection coefficient at grain boundaries.

Fig. 7: The median grain sizes and the electrical resistivity for different line widths are compared for samples subjected to standard post-plating annealing or RTA.
Further investigations regarding the reflection coefficient at grain boundaries in Cu interconnects are needed in order to study its influence on the electrical resistivity.

**Conclusions**

Grain size engineering is one option to reduce the size effect related resistivity increase. Additional annealing after processing is insufficient in order to enhance a second recrystallization process. For temperatures higher than 500°C hillocks are formed. Only high temperature rapid thermal annealing leads to larger grains in particular in wide lines. For ultrafine Cu lines with AR>1 the microstructure advantage leading to a lower resistivity is less effective. The median grain size at deep-100 nm level is mainly determined by the geometry dimension of the line and cannot be significantly influenced by different annealing conditions. As a result, even for different annealing conditions the resistivity increase of ultrafine interconnects (<100 nm) must be seriously taken into account for characterization of future metallization systems.

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**References**