Measurement of Adhesion Strength in Copper Interconnection Layers

Tohru Hara, Minoru Uchida, Masayo Fujimoto, Toshiro K. Doy, Subramanian Balakumar, and Narayanan Babu

*Department of Electrical Engineering, Hosei University, Koganei, Tokyo 184-0002, Japan
*a Saitama University, Urawa, Saitama 338-8570, Japan
*Institute of Microelectronics, Science Park II, 117685 Singapore

The adhesion strength of copper layers on TaN barrier layers decreases from 19.5 to 10 gf with annealing at 400°C. A much lower stress layer can be obtained when a seed layer is deposited on a TaSiN barrier layer. The adhesion strength is as high as 35 gf and is not changed by annealing. The critical pressure for delamination at the barrier layer/low dielectric layer interface decreases from 350 to 200 g/cm² when e is reduced from 3.3 to 2.7 in an SiOC interlayer. That is, better adhesion strength can be attained when an interlayer with a higher dielectric constant is used.© 2003 The Electrochemical Society. [DOI: 10.1149/1.1635092] All rights reserved.

Copper and low dielectric (e) interlayers have been used extensively as multilevel interconnections for the enhancement of speed in logic large-scale integrated circuits (LSIs). However, delamination and peeling frequently occur during chemical mechanical planarization (CMP) in highly stressed copper interconnection layers deposited on Ta and TaN barrier layers. Delamination and void formation occur to release the stress, particularly when annealing is done for highly stressed copper layers. Therefore, CMP must be carried out at lower pressures and lower removal rates, which are usually designated empirically. Enhancement of the removal rate has been achieved in practical terms by employing an additive in the slurry to form a brittle layer at the copper surface. The formation of scratches and the occurrence of dishing are serious problems in the CMP process for copper layers. However, it has been believed that this is a problem merely of vendors, polishing machines, and consumables. Therefore, few researchers have shown interest in delamination, although it has become a serious problem.

Recently, it was reported that the adhesion strength and layer properties of electroplated copper layers are determined mainly by the stress in the seed layers that are used for electroplating. A barrier layer consisting of a Ta/TaN bilayer has been used extensively for multilayer copper interconnections. Because this is a typical high stress copper layer, some reduction of stress is required for CMP. Enhancement of the adhesion strength in layers has been attained by the formation of low stress copper interconnects. Recently, it was reported that the adhesion strength and critical pressure for delamination are lower at the barrier/low-e interlayers than they are for Cu/barrier layers after a manufactured low stress copper layer. Therefore, delamination occurs frequently at the barrier layer/low-e interlayer, specifically in the bevel area of the wafer when employing a low-e interlayer instead of a chemical vapor deposition (CVD) SiO₂ interlayer in the CMP. However, quantitative measurements of adhesion strength have not been carried out at this interface until now. The polishing rate is so low for conventional barrier layers, such as Ta and TaN, that CMP must be carried out at higher pressures, but then delamination occurs easily at the barrier layer/low-e interlayer. Therefore, enhancement of the adhesion strength is required to establish higher speed CMP without delamination occurring. This paper describes the quantitative measurement of adhesion strength and critical pressure for delamination at the copper/barrier layer interface and at the barrier layer/low-e interlayer.

---

Experimental

SiOC interlayers were deposited at 350°C in a parallel-plate radio-frequency (rf) plasma-enhanced (PECVD) reactor manufactured by Applied Materials. The plasma was sustained with an rf power generator operating at 13.56 MHz. The process gases, consisting of trimethylsilane [SiH(CH₃)₃], referred to as 3MS) and oxygen were fed into the reactor, where the 3MS/O₂ gas flow rate ratio was held at 6. Here, (100) oriented p-type (boron-doped) silicon wafers with a diameter of 200 mm were used as substrates. Layers were deposited using the following three sets of conditions, under a continuous power mode using different pressures at a pressure of 4 Torr. The deposition powers and the growth rates were:

- Layer 1: Power: 100 W, growth rate: 105 nm/min, C: 0.15, dielectric constant: 2.7
- Layer 2: Power: 600 W, growth rate: 680 nm/min, C: 0.25, dielectric constant: 3.0
- Layer 3: Power: 1200 W, growth rate: 1549 nm/min, C: 0.30, dielectric constant: 3.3

A copper seed layer (30 nm thick) was deposited by magnetron sputtering and a 300 nm thick copper interconnection was electroplated on the seed layer employing a conventional copper sulfate electrolytic solution.

Results and Discussion

Cu layer.—Delamination and peeling frequently occur during CMP for highly stressed copper interconnection layers deposited on conventional barrier layers of Ta/TaN and TaN. Therefore, CMP must be carried out at low pressures and at low removal rates to solve this problem. However, stress relaxation of the copper layers cannot be accomplished by this process. Researchers have been forced to use highly stressed fine copper interconnection lines in the manufacture of LSIs. This stress tends to be released by migration and by the formation of voids during the operation of LSIs when a high current density is flowing into fine lines. Electromigration resistance is the most important advantage in copper interconnections. This advantage is loose when such a high stress line is used. Improvements in electromigration resistance can be attained only by depositing low stress copper interconnection layers. Enhancement of adhesion strength can be achieved also by deposition of a low stress interconnection layer.

Stress measurements were performed for electroplated copper layers deposited on conventional TaN barrier layers. The variation of the stress with annealing is shown in Fig. 1, where the open and closed triangles represent data before and after annealing at 400°C. The stress was as high as 33 MPa in the as-deposited copper layers. Although slightly lower stress was obtained for layers on a Ta barrier layer, Ta is typically a poor barrier layer with respect to copper diffusion. The stress decreased to 24.5 MPa after this annealing step.

---

* Electrochemical Society Active Member.
4 E-mail: hara@k.hosei.ac.jp
Reportedly, this marked reduction in stress is due to the formation of voids in the copper layer. Figure 2 illustrates the surface features of the annealed copper layer (200 nm thick) using a scanning electron microscopy (SEM) photograph. Voids were not observed clearly at the surface in the as-annealed layer, although many voids were formed at the grain boundaries with this stress relaxation. However, voids were observed clearly and quantitatively after performing grain boundary etching by employing a recently developed electrolytic etching process. The voids are surrounded by open circles in Fig. 2. Such voids can be formed among the grains by stress relaxation as seen in Fig. 2. The density of the voids was $2 \times 10^7 \text{ cm}^{-2}$ at the surface of this layer and increased markedly when approaching the interface with the barrier layer. The density and the area of the voids are proportional to the amount of stress released by the void formation.

Figure 1 also shows the correlation of adhesion strength with stress in the copper seed layer for as-deposited layers. Adhesion strength decreases perceptibly from 19.5 to 10 gf with a marked reduction in stress with this annealing. Adhesion strength in the as-deposited copper layers decreases with the increase of stress. However, this relationship was no longer valid in the layer after annealing. This is because the adhesion strength decreased markedly due to the formation of voids after annealing. The stress was as low as 26 MPa in a low stress copper layer electroplated under much the same conditions on a low stress seed layer. The adhesion strength remained at around 40 gf after annealing as shown by the closed circle in Fig. 1, because such a high degree of stress relaxation was no longer needed in this low stress layer. These results highlight the importance of depositing low stress copper interconnection layers to achieve better adhesion strength.

The structure of the copper interconnection layer that we employed to observe the quantitative adhesion strength at the Cu/barrier and the barrier/interlayer interface is shown schematically in Fig. 3, where a low-$\sigma$ SiOC and a conventional CVD SiO$_2$ interlayer were used. After depositing the different barrier layers, such as TaN, Ta/TaN, and TaSiN, on SiOC interlayers, a 30 nm thick copper seed layer and a 300 nm thick interconnection layer were deposited by magnetron sputtering and by electroplating, respectively. The adhesion strength and the stress were determined quantitatively by scratch testing and by the shift angle in the X-ray diffraction spectra. Here, a high stress layer means a conventional copper interconnection layer and a low stress layer means a low stress seed layer formed by the agglomeration process. Figure 4 explains the variation in adhesion strength of the electroplated copper layer (as-deposited) with the stress in the copper seed layer for as-deposited copper interconnection layers, where the stress was controlled by varying the barrier layer. Figure 4 shows that the adhesion strength in the copper interlayer is closely related with the stress in the seed layer employed for electroplating. That is, higher stress and lower adhesion strength were obtained at the Cu/barrier layer in conventional copper interconnection layers on Ta/TaN and TaN barrier layers. The stress decreased markedly and the adhesion strength increased to 35 gf in the layer deposited on a TaSiN barrier layer. This stress is much higher than 25 and 30 gf in the layer on Ta/TaN barrier layers. This is because a lower stress seed layer can be deposited on a TaSiN barrier layer as reported elsewhere. The critical pressure for delamination was determined for this interconnect deposited on the TaN barrier layers. The critical pressure is defined as the minimum pressure at which delamination appeared, where in which the polishing pressure was increased gradu-
barrier layer and a TaSiN (low stress) layer were deposited on CVD SiOC interlayers with different dielectric constants. The critical pressure and the adhesion strength are not affected by the particular kind of barrier layer that was used. This pressure is mostly controlled by the dielectric constant of the SiOC interlayer. That is, the critical pressure decreased perceptibly with decreasing dielectric constant and adhesion strength at this interface. Here, the critical pressures for peeling were high and ranging at 360 g/cm² at the barrier layer/interlayer when conventional CVD SiO₂ and CVD SiOC (ε: 3.3) interlayers were employed. Delamination is not a problem at this interface. However, the critical pressure decreased rapidly with decreasing dielectric constant and reached 200 g/cm² in the layer with a dielectric constant of 2.7 as seen in Fig. 5. This pressure decreased further with annealing and reached 120 g/cm² when this sample was annealed at 400°C. This pressure is comparable with that at the interface of a conventional high stress copper layer. Delamination occurs at low pressure during CMP of the barrier layer when a low-ε SiOC interlayer is used. A higher critical pressure can be attained at this interface only when a higher dielectric constant interlayer, for instance, above 3.3, is used. The critical pressures that we have observed are shown numerically in Fig. 3.

Conclusions

Highly stressed copper interconnection layers were deposited on conventional TaN barrier layers. This stress can be decreased from 33 to 24.5 MPa by annealing at 400°C. This stress reduction is due to the formation of voids at the grain boundary. Therefore, the adhesion strength decreased from 19.3 to 10 gf due to this stress relaxation. The adhesion strength is much higher in a layer deposited on a low stress seed layer, which remained at 40 gf after annealing. Delamination occurs at low polishing pressure in such a low adhesion layer.

The adhesion strength of the copper layer decreased with reducing stress in the seed layer employed for electroplating. This stress can be controlled by the barrier layer. The adhesion strength of the copper layer is less affected by the dielectric constant of the CVD SiOC interlayer.

The critical pressure for delamination at the barrier layers deposited on the different interlayers showed that the critical pressure is weakly dependent on the barrier layer. The critical pressure for a copper layer decreased rapidly from 350 to 200 g/cm², as the dielectric constant of the interlayer decreased from 3.3 to 2.7. Enhancement of the critical pressure at the TaN/SiOC interlayer can be achieved by increasing the dielectric constant in the low-ε interlayer.

Acknowledgment

We are much indebted to Dr. R. Kumar at the Institute of Micro-electronics in Singapore for his technical support.

Hosei University assisted in meeting the publication costs of this article.

References