ELSEVIER

Microelectronic Engineering 50 (2000) 473–479

MICROELECTRONIC ENGINEERING

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Room temperature electroless plating copper seed layer process for damascene interlevel metal structures

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Abstract

Described in this paper is the development of a room temperature electroless copper seed layer deposition process on ultra-thin TiN barrier layers. This novel process is compatible with damascene interlevel metal structures for sub-0.18 micron ULSI processes. An optimum copper layer thickness of 50 nm and a deposition rate of 45 nm min^{-1} was targeted and obtained. Atomic force microscopy (AFM) reveals that the non-uniformity of the seed layer is less than 10% of the film thickness, while four-point probe measurements indicate that the resistivity of the copper seed layer is less than 6 $\mu\Omega\ cm^{-1}$. Secondary ion mass spectroscopy (SIMS) reveals that potential metallic contaminants such as sodium, potassium, calcium and magnesium ions do not penetrate the TiN barrier layer. Rutherford back scattering (RBS) indicates that the palladium concentration in the seed layer is approximately 1%, which is low enough to avoid wafer contamination and increased resistivity in the subsequent electroplated copper layer.

Keywords: Electroless; Copper; Seed layer; Plating; Damascene

1. Introduction

The 0.18 micron ULSI technology generation marks a paradigm shift in CMOS fabrication technologies. The increasing number of interconnect metal levels requires a planar technology, therefore approaches to the fabrication of copper–damascene interconnection structures are currently of high interest [1,2]. The trend towards further miniaturisation of integrated circuits and the high costs associated with copper-CVD and PVD technologies has led to the search for alternative means of metal deposition. The recent interest in Cu-based metallisation for ULSI devices has stimulated extensive studies on the search for novel deposition and etching processes [3].

Electroless metal deposition is under increased investigation as an alternative to conventional techniques due to its low cost, the relatively low processing temperatures involved and the ease of

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0167-9317/00/$ – see front matter
PII: S0167-9317(99)00317-2

implementation [4]. Due to improvements in photolithographic technologies ever smaller line widths and higher aspect ratio trenches are being produced, and so electroless copper deposition becomes an ever more attractive means for yielding conformal, high quality seed layer copper metallisation. The properties of these chemically deposited copper coatings, such as high conductivity and low resistivity, make them suitable as seed layers for metallisation of dielectric materials prior to subsequent thick electroplating [5].

In this contribution, we report on the development of a room temperature electroless plating copper seed layer process for damascene interlevel metal structures on ultra-thin TiN barrier layers for sub-0.18 micron ULSI processes. This current approach builds on previous work using electroless copper plating of vias for 0.25 micron CMOS [6,7] and explores a potentially low-cost alternative to Cu-CVD and PVD.

2. Experimental

All experiments were carried out on eight-inch diameter TiN wafers. The TiN was deposited by CVD using a TDMAT precursor provided by a bubble source. A reactive N_2/H_2 plasma treatment was performed for 40 s and a layer thickness of 100 Å produced. The deposition and plasma treatment process was repeated to produce a final TiN thickness of 200 Å. The pressure was 1 T both during deposition and plasma treatment. The aqueous activating solution consisted of a palladium salt and hydrofluoric acid. Activated substrates were plated in a commercial electroless copper bath (Alfachimici Cuprosure '93) at a temperature of 25°C with continuous agitation.

Titanium nitride thicknesses were obtained using a Jobin-Yvon ISA UVISEL phase modulated variable angle surface ellipsometer (VASE). Atomic force microscopy was performed using a Topometrix Explorer TMX 2000 atomic force microscope in contact and non-contact mode. Scanning electron microscopy was carried out using a Hitachi S4000 field emission scanning electron microscope equipped with a Princeton Gamma Technology energy dispersive spectrometer. Copper thickness measurements were obtained using a Tencor AS400 profilometer. Resistivity measurements were made using a four-point probe on a Prometrix Omnimap RS35e system. Secondary ion mass spectroscopy was carried out using a standard CAMECA IMS 3F ion microscope with both liquid metal (caesium) and gas duoplasmatron (argon or oxygen) primary ion sources. Adhesion of copper deposits was examined using standard tape and scratch tests.

3. Results and discussion

To ensure reliability and to successfully integrate copper as an interconnecting layer, it is necessary to develop a diffusion barrier with the capacity to prevent copper migration into SiO_2. Titanium nitride (TiN) is one of several materials that show attractive characteristics such as low bulk resistivity and high thermal stability. These properties make it compatible to semiconductor technology and it has already been successfully employed as a diffusion barrier between aluminium and its alloys and silicon [8].

3.1. Initiation of electroless copper deposition

TiN forms a protective oxide, TiO_2, on exposure to air. This oxide can be removed by dipping the substrate into an etching solution, normally consisting of strong acids. However, TiN has a high affinity for oxygen and any exposure to air will cause the immediate regrowth of oxide causing poor adhesion of the deposited copper. Therefore, conventional methods of alkaline cleaning or acid etching are insufficient for titanium alloys. Patterson et al. have recently demonstrated a suitable pre-treatment that involved both removal of the TiO_2, using HF, and activation of the TiN surface, with Pd, in one step prior to plating [6].

Using a similar method, we have successfully etched and activated TiN barrier layers using a Pd/HF solution [6]. HF in the activation solution removes oxide from the TiN surface and continues to etch the TiN barrier layer while at the same time the palladium seed layer required for the autocatalytic reaction is deposited as follows:

$$Ti^0 + 6HF \rightarrow H_2[TiF_6]_{aq} + 2H_2\uparrow + 4e^- \quad (1)$$

$$Pd^{2+} + 2e^- \rightarrow Pd\downarrow \quad (2)$$

An etch rate of 25 Å min^{-1} was measured for the TiN using VASE. Therefore, in order to obtain a 100 Å TiN diffusion barrier layer after a 4 min activation time, an initial TiN thickness of 200 Å was required. Fig. 1 shows a SEM of an activated TiN barrier layer. The Pd ions are reduced to metal and distributed in a random fashion on the TiN surface. The island-like structure provides the platform for a continuous electroless copper seed layer on the TiN barrier layer.

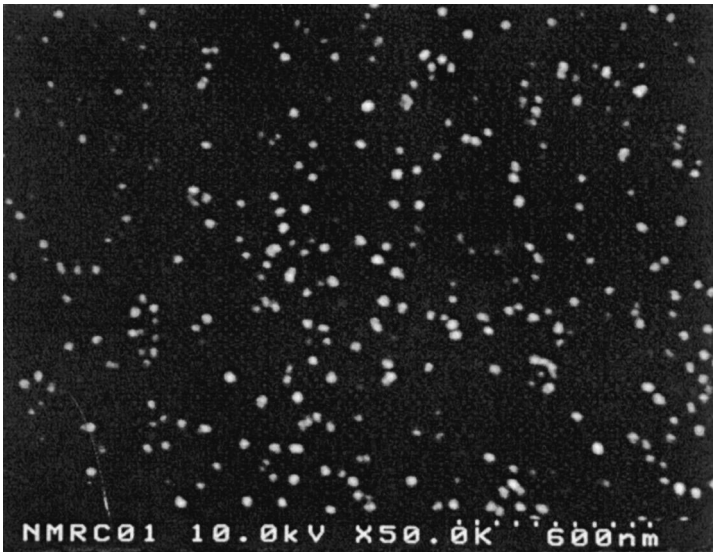

Fig. 1. SEM of titanium nitride surface on a patterned wafer after immersion in HF/Pd activation solution for 4 min.

3.2. Uniformity and plating rate of electroless copper seed layers

Initial experiments investigating the electroless deposition of copper onto activated TiN barrier layers were aimed at producing continuous, uniform copper films. Uniform electroless copper films have previously been produced by employing 1 h deposition times [7]. In this paper, we report on the development of a plating process that results in a flash electroless copper seed layer process for sub-micron CMOS processing applications. Fig. 2 shows a SEM of a horizontal feature on a patterned wafer after electroless copper deposition. The particle size of the copper on these wafers is approximately 50 nm and Fig. 2 reveals that a smooth continuous coverage of the horizontal features has been achieved. This is confirmed by the AFM analysis shown in Fig. 3, which shows a continuous copper seed layer with a roughness value, R_a, of 3.1. This represents a non-uniformity of less than 10% of the film thickness, which is 50 nm. The plating rate measured using profilometry and SEM has been determined to be 45 nm min^{-1}.

Further examination of patterned features using SEM and AFM reveal that, while all horizontal features on patterned wafers were plated with a continuous, smooth layer of copper, the side wall coverage is not as efficient. As Fig. 4 illustrates, the coverage of the side wall is approximately 75%. Problems associated with via holes of 230 μm diameter and less (aspect ratio 2.3:1) have been reported [9]. In these cases the agitation of the plating solution is suppressed with the reduction in the size of the via. However, 100% coverage of all horizontal features on our wafers suggests decreased agitation does not explain the origin of the observed results.

The difference in coverage between the horizontal and vertical features appears to be a result of the manner in which the TiN has been deposited. The TiN has been N_2/H_2 plasma treated in a vertical fashion so that the TiN on the planar features receives more plasma treatment than the vertical features. Therefore, the TiN on the horizontal and vertical features is structurally different, and so the

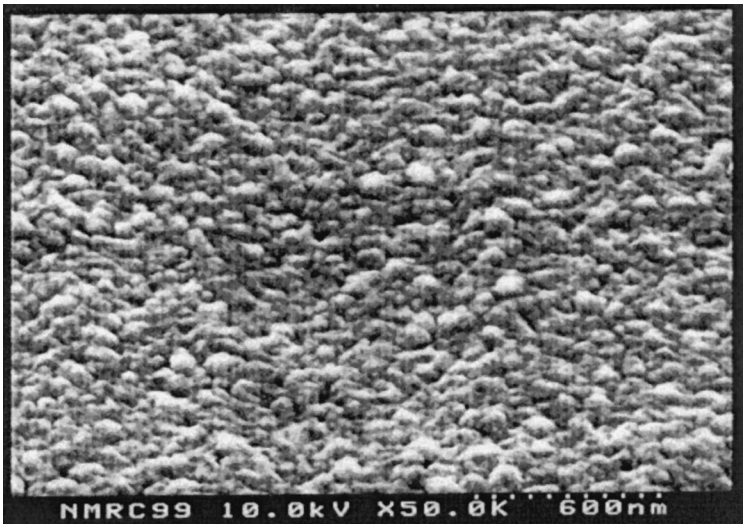

Fig. 2. SEM of a horizontal feature on a patterned wafer after electroless copper plating.

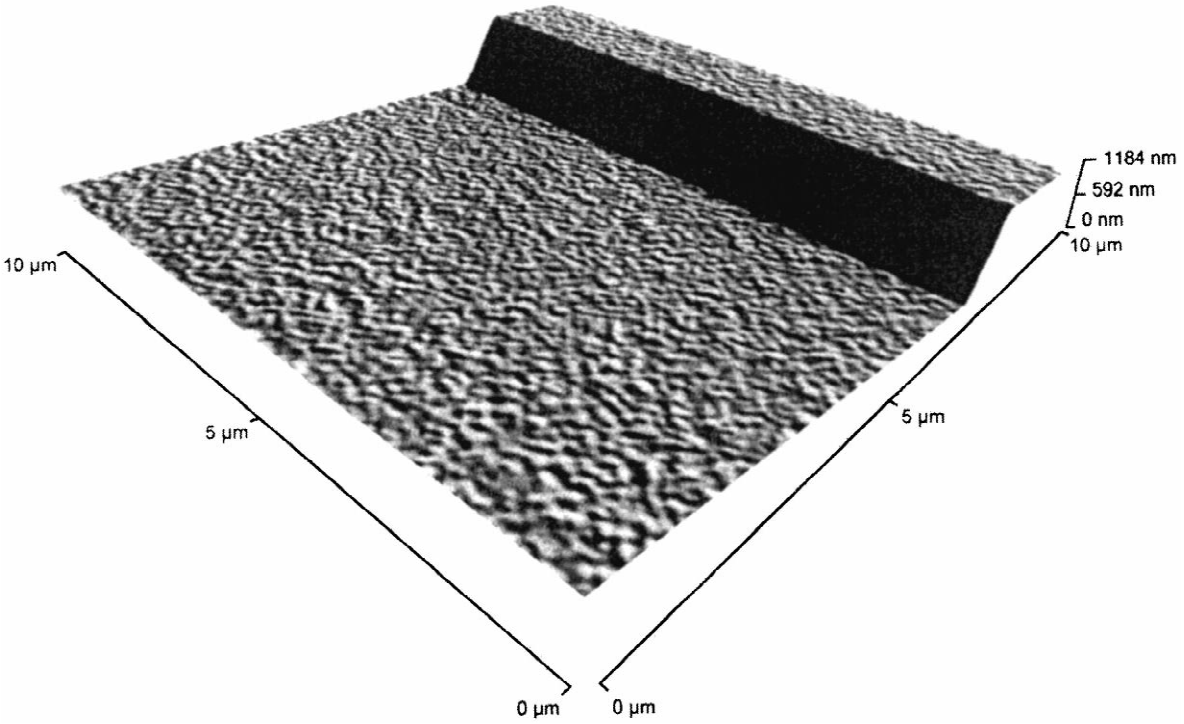

Fig. 3. AFM of a patterned wafer after electroless copper deposition.

plating rates for the side walls and planar features are different. This variance in plating rate has been confirmed by studying unpatterned plasma and non-plasma-treated wafers. The plating rate for plasma-treated wafers was approximately 35 nm min^{-1}, while that for non-plasma-treated wafers was approximately 15 nm min^{-1}. This may account for the difference in uniformity between the horizontal and vertical features.

3.3. Resistivity and adhesion

A major advantage of copper over aluminium for use in microelectronics is its low resistivity and improved electromigration properties and for this reason it is becoming the interconnect metal of choice in CMOS architectures and fabrication. We have used a four-point probe to determine resistivities of our copper seed layers. For a 50 nm thick electroless copper seed layer, a resistivity of 5.8 $\mu\Omega\ cm^{-1}$ was obtained. This resistivity is quite low for a copper seed layer that has an underlying Pd sublayer and suggests that the concentration of Pd is low and that the structure of the seed layer is uniform [5]. Rutherford back scattering confirms that the concentration of Pd in the copper seed layer after electroless copper deposition is 1%.

The adhesion of the electroless copper seed layers was tested using the Scotch tape and scratch tests. All electroless copper deposits up to a thickness of 50 nm passed tape and scratch tests.

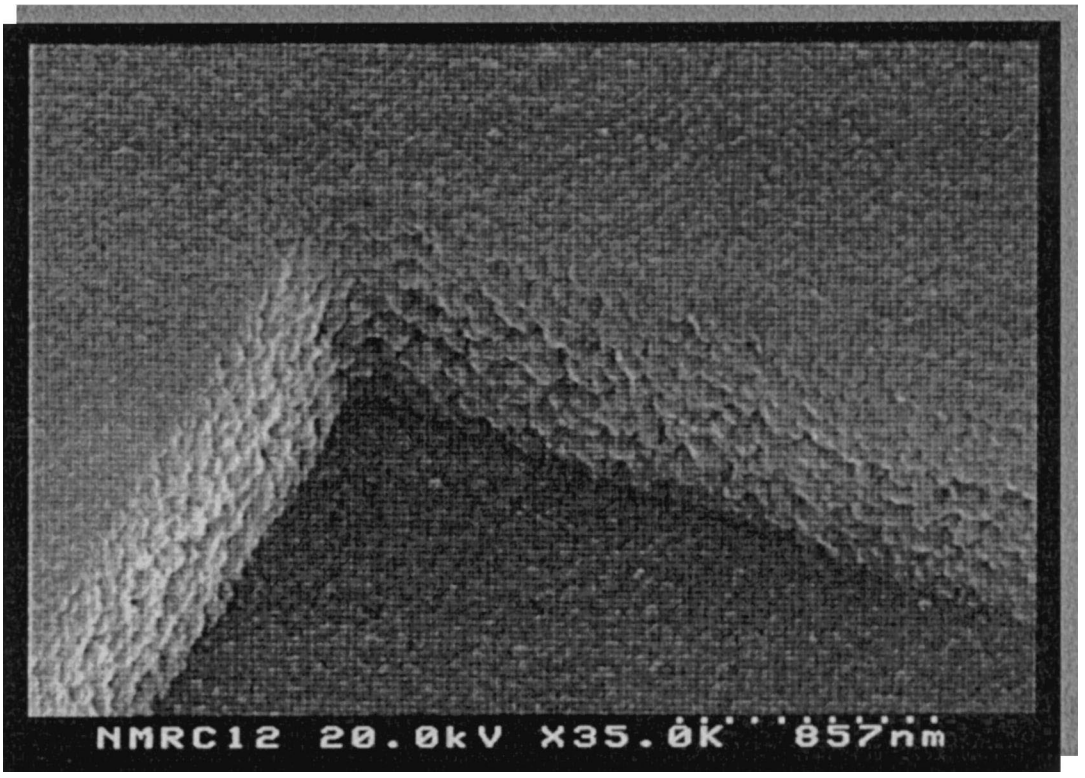

Fig. 4. SEM of a 200 mm patterned wafer after electroless deposition showing full coverage of horizontal features and 75% coverage of side walls.

3.4. Contamination studies

Conventional electroless copper deposition solutions include several components that are considered major contaminants for integrated circuit manufacturing. The most obvious contaminant, sodium, arises from the high concentrations of sodium hydroxide that are used to produce the high pH of the electroless solutions. Sodium contamination may undermine the long-term stability of integrated circuits and, as we have employed electroless copper plating baths that use sodium hydroxide, it is necessary to determine if adulteration of the SiO_2 occurs. Secondary ion mass spectroscopy has been employed to determine the concentrations of sodium in plated wafers. Depth profiles reveal that while small quantities of sodium, potassium, calcium, and magnesium are present in the deposited copper layer, diffusion of these ions through the TiN diffusion barrier into SiO_2 does not occur over time.

4. Conclusion

Room temperature, electroless copper seed layers have been produced on patterned eight-inch diameter wafers having titanium nitride barrier layers. Horizontal features of various widths down to 0.3 μm have been successfully plated. Although only 75% coverage has been obtained on side walls,

this may be adequate for further electroplating of the wafers. Copper seed layers can be deposited with good adhesion up to a thickness of 50 nm with a plating rate of 45 nm min^{-1}. These room temperature seed layer deposits are compatible with ULSI technology for interconnect manufacturing of eight-inch wafers and represent an important step toward full copper–damascene interconnect deep sub-micron ULSI.

Acknowledgements

Financial support under EU ESPRIT project 25220, Damascene, is gratefully acknowledged.

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