1. Doctor J needs a PWM output signal with a PWM period of 25 ms and a duty cycle of 85%. His timer is clocked by the 10 MHz peripheral bus clock with a clock prescale of 4. Help Poor Dr. J configure both Timer 2 and Output Compare module 3 so he can complete his lab and go home!
2. What is the data rate above in bits per unit time, e.g., how many bits per PWM period?
3. Joe Vandal appears in the lab and starts to pose questions to the poor doctor:
	1. What will happen to the PWM signal if you double the value in OC3R?
	(i.e., fPWM, duty cycle, resolution, and THI)
	2. What will happen if you instead use a timer prescale of 1?
	3. How about if you instead double (PR2+1)?