# ECE 440 AXI Traffic Generator to Stream FIFO to Factorial

Please answer the following “Yes” or “No”

1. Did you create and validate a block diagram with all components instantiated (Traffic Generator, Stream FIFO, Custom IP)?
2. Does the design synthesize cleanly without any errors?
3. Were you able to perform a post-synthesis simulation?
4. Were the results correct?

Additional Information:

Include post-synthesis timing simulations and upload this document as a PDF file to Canvas.