# ECE 440 Factorial Co-Processor

Please answer the following “Yes” or “No”

1. Does your factorial project (not IP) synthesize cleanly and simulate correctly?
2. Do the factorial IP and AXI slave IP package correctly without errors?
3. Did you create and validate a block diagram with the AXI slave and factorial IP instantiated?
4. Does the design build cleanly and export the hardware from Vivado without errors?
5. In the SDK, were you able to create a BSP with the appropriate drivers?
6. Were you able to compile and run your C code?
7. Did anything appear in the SDK terminal window?
8. Was it correct?

Additional Information: